INTEGRATED POWER DEVICE WITH IMPROVED EFFICIENCY AND REDUCED OVERALL DIMENSIONS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention refers to an integrated power device, and more particularly to an IGBT with control circuit having improved efficiency and reduced overall dimensions.

Description of the Related Art

As is known, power devices are used in all applications that require handling of high voltages and currents.

For example, Figure 1 shows an integrated power device 1 comprising a power transistor 2, built using an insulated-gate bipolar transistor (IGBT), and a control circuit, which may, for example, be made as described in the European patent application No. 00830051.9 filed on January 27, 2000 in the name of the present applicant. More specifically, the power transistor 2 has a collector terminal on which a high collector voltage Vc (for example 300 to 400 V) is present, an emitter terminal connected to a ground line GND set at a ground voltage V_{GND}, and a control terminal connected to an output terminal 3a of the control circuit 3.

In turn, the control circuit 3 comprises an input terminal 3b for receiving a driving signal S, a supply terminal 3c set at a supply voltage V_B (for example, of from 6 to 24 V), a ground terminal 3d connected to the ground line GND, a sensing terminal 3e connected to the collector terminal of the power transistor 2, and a feedback terminal 3f connected to the emitter terminal of the power transistor 2 via a voltage-to-current transducer 4.

The control circuit 3 receives the driving signal S and controls turning-on and turning-off of the integrated power device 1. In addition, it carries out a control on the

value of the collector voltage Vc, detected by the sensing terminal 3e, for example by blocking the collector voltage Vc at a value programmed according to the operating conditions of the integrated power device 1, or else by stabilizing the oscillations of the collector voltage Vc during transients, or yet again by controlling the value dVc/dt. The control circuit 3 also controls the value of the current Ic flowing in the power transistor 2. The current Ic is detected by the voltage-to-current transducer 4, which supplies it to the control circuit 3 via the feedback terminal 3f. In this case, the control circuit 3 carries out a control on the current Ic, for example by controlling the value dIc/dt, or else by preventing the current Ic from exceeding a maximum value beyond which the integrated power device 1 may be subject to failure.

At present, there exist two possible solutions for assembling the integrated power device 1 described above.

In a first solution (chip-to-chip solution), shown in Figure 2, a first chip 60 and a second chip 62, which respectively integrate the power transistor 2 and the control circuit 3 (of which Figure 2 shows only one portion), are soldered on one and the same copper plate 5. In this first solution, the control circuit 3 is made using an M1-type technology, which enables integration, in a high-voltage region (*i.e.*, one able to withstand high voltages, for example 500 V), of components operating at low voltages (for example, 40 V).

In greater detail, the first chip 60 comprises a first substrate 6, of the P type, soldered on a first portion 5a of the copper plate 5 and defining a collector region of the power transistor 2. A first epitaxial layer 7, of the N^+ type, is grown on top of the first substrate 6, and a second epitaxial layer 8, of the N^- type, and having a surface 8a, is grown on top of the first epitaxial layer 7. Body regions 9, of the P^+ type, are housed in the second epitaxial layer 8, are set facing the surface 8a, and in turn house emitter regions 10, of the N^+ type, set apart from one another by means of respective portions 9a of the body regions 9.

Polysilicon gate regions are set between pairs of body regions 9, on top of the surface 8a, and are electrically insulated from the latter by a gate-oxide layer 12. A

thick oxide layer 13 envelops the gate regions 11 and separates them electrically from a metal emitter-contact region 14, which extends on top of the chip 60 and is in electrical contact with the emitter regions 10 and with the portions 9a of the body region 9 by means of contact portions 14a.

The second epitaxial layer 8 also houses an edge structure 15 of the power transistor 2 comprising a first annular region 16, a second annular region 19, and an equipotential portion 8′ belonging to the second epitaxial layer 8 and facing the first annular region 16 and the second annular region 19. The first annular region 16, of the P^- type, completely surrounds the area in which the body regions 9 are formed (active area 17) and is overlaid by a thick field-oxide layer 18. The second annular region 19, of the N^+ type, surrounds the first annular region 16 externally (Figure 3) and forms a channel stopper.

A field-plate region 20 extends on top of the active area 17 and is electrically insulated from the surface 8a of the second epitaxial layer 8 by the gate-oxide layer 12. A Zener diode 21 extends in part over the field-oxide layer 18 adjacent to the field-plate region 20. The field-plate region 20 and the Zener diode 21 are formed starting from one and the same polycrystalline-silicon layer.

The Zener diode 21 has a first end 21a and a second end 21b. The first end 21a is in electrical contact with a metal gate-contact region 22, which is set outside the active area 17 (Figure 3), whilst the second end 21b is in electrical contact with a first contact portion 23a of a metallization region 23. The metallization region 23 has a second contact portion 23b which is in electrical contact with the equipotential portion 8′, as schematically represented in Figure 2, via an intermediate node 24 connected to the collector region 6 through a first diode 25, and to the metal emitter-contact region 14 through a second diode 26.

In particular, the first diode 25 has a cathode region defined by the first epitaxial layer 7 and an anode region defined by the collector region 6, whilst the second diode 26 has an anode region defined by the body region 9 and a cathode region defined by

the epitaxial layer 8. The first diode 25 and the second diode 26 are connected together in antiseries via the intermediate node 24.

The second chip 61 comprises a high-voltage region 30 which is bonded on top of a second portion 5b of the copper plate 5, adjacent to the first portion 5a. The high-voltage region 30 is electrically connected to the collector region 6 of the power transistor 2 by means of the copper plate 5 and is formed by a second substrate 31, of the N^+ type, directly bonded on the second portion 5b of the copper plate 5, and a third epitaxial layer 32, of the N^- type, grown on top of the second substrate 31 and having a surface 32a. The third epitaxial layer 32 houses an insulation region 33, of the P type, delimiting a first portion 32b and a second portion 32c of the third epitaxial layer 32, in which a first bipolar transistor 34, of the PNP type, and a second bipolar transistor, of the NPN type, which operate at low voltage, are respectively made.

More specifically, the first bipolar transistor 34 comprises a buried base region 36, of the N^+ type, formed on top of the isolation region 33 and extending in part into the latter, and a deep base region 37, also of the N^+ type, which extends from the surface 32a of the third epitaxial layer 32 as far as the buried base region 36 so as to connect the latter electrically to the surface 32a itself. Above the buried base region 36 and at a distance from the latter are a first surface region 38, a second surface region 39, and a third surface region 40, all of the P type. The first surface region 38 and the third surface region 40 define an emitter region of the first bipolar transistor 35, whilst the second surface region 39 defines a collector region. On top of the surface 32a are a first metal region 41, a second metal region 42, a third metal region 43, a fourth metal region 44, and a fifth metal region 45, which are in electrical contact, respectively, with the first isolation region 33, the first surface region 38, the second surface region 39, the third surface region 40, and the deep base region 37. The second metal region 42 and the fourth metal region 44 together define an emitter-contact region of the first bipolar transistor 34; the third metal region 42 defines a collector-contact region of the first bipolar transistor 34; and the fifth metal region 45 defines a base-contact region.

In turn, the second bipolar transistor 35 comprises a buried collector region 46, of the N^+ type, formed on top of the isolation region 33 and extending in part into the latter, and a deep collector region 47, also of the N^+ type, which extends from the surface 32a of the third epitaxial layer 32 as far as the buried collector region 46 so as to connect the latter electrically to the surface 32a itself. Above the buried collector region 46 and at a distance from the latter is a base region 58, of the P type, housing a surface emitter region 49, of the N^+ type. On top of the surface 32a are a sixth metal region 49, a seventh metal region 50, an eighth metal region 51, and a ninth metal region 52, which set in electrical contact, respectively, the base region 42, the surface emitter region 48, the deep collector region 46, and the insulation region 33. The sixth metal region 49 defines a base-contact region of the second bipolar transistor 35; the seventh metal region 50 defines an emitter-contact region of the second bipolar transistor 35; and the eighth metal region 51 defines a collector-contact region.

Although the chip-to-chip solution described above is advantageous from various points of view, it presents, however, some drawbacks when the collector terminal of the power transistor 2 is connected to the terminal of a primary winding of an ignition coil. In these conditions, in fact, the ignition coil, after storing the amount of energy necessary for producing an ignition spark, returns part of this energy (discharge phase), generating on its own primary-winding terminal, and hence on the collector terminal of the power transistor 2, a voltage which is negative with respect to the ground voltage V_{GND}. This negative voltage, via the copper plate 5, is applied to the high-voltage region 30. Consequently, when the value of the negative voltage reaches the maximum value of the reverse voltage of insulation of the control circuit 3, a high current is injected into the high-voltage region 30. This current may prove destructive for the control circuit itself.

At present, in order to absorb the energy returned by the ignition coil and prevent destruction of the control circuit 3, a first protection diode 54 and a second protection diode 55 (shown in Figure 1 by a dashed line) are connected together in antiseries between the collector terminal of the power transistor 2 and the emitter terminal.

However, the use of these external components involves an increase in the area occupied by the integrated power device 1 and in the costs for fabrication of said device.

In order to overcome this problem, a second known solution (chip-on-chip solution) envisages implementation of the control circuit 3 using BCD or CMOS technologies, which employ substrates operating at low voltages (for example, 40 V); next, the control circuit 3 is bonded on the metal emitter-contact region 14 of the power transistor 2.

In this case, the control circuit 3 is protected from the negative voltage peaks to which the collector terminal of the power transistor 2 is subject, since it is completely insulated from the latter. In these conditions, however, the control circuit 3 is not able to perform control of the collector voltage Vc, which proves of fundamental importance when the integrated power device 1 is used for driving an ignition coil.

BRIEF SUMMARY OF THE INVENTION

The disclosed embodiments of the present invention are directed to an integrated power device with improved efficiency and reduced overall dimensions, that includes a power component, ideally an insulated gate bipolar transistor, having a first high-voltage region, a low-voltage region, a first unidirectional element and a second unidirectional element connected together between the first high-voltage region and the low-voltage region, the first and second unidirectional elements defining a common intermediate node; a biasing circuit connected between the common intermediate node and the second high-voltage region; and a control circuit that includes a high-voltage region.

In accordance with another aspect of the foregoing embodiment, the biasing circuit includes a contact pad electrically connected to the common intermediate node, an electrical connection region formed on the second high-voltage region, and an electrical connection line having a first end connected to the contact pad and a second end connected to the second electrical connection region.

In accordance with another aspect of the foregoing embodiment, the power component includes an edge structure, and the contact pad is set on top of the edge

structure, with the edge structure ideally being formed of an equipotential annular region surrounding the power component, and the contact pad is set on top of the equipotential annular region.

In accordance with another embodiment of the present invention, the power component is formed on a first chip and the control circuit is formed on a second chip that is set on top of and affixed to the first chip, the second chip including a substrate fixed to the low-voltage region by means of an adhesive layer.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

The characteristics and advantages of the integrated power device formed in accordance with the invention will emerge from the ensuing description of a representative of embodiment, which is given to provide a non-limiting illustration, with reference to the attached drawings, in which:

Figure 1 shows a simplified diagram of an integrated power device;

Figure 2 shows a cross section of the integrated power device;

Figure 3 shows a plan view of a power portion of the integrated power device;

Figure 4 shows an integrated power device connected to an ignition coil;

Figure 5 shows a cross section of an integrated power device made according to the present invention; and

Figure 6 shows a plan view of the integrated power device of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

Figure 4 shows an integrated power device 100 connected to an ignition coil 101. To the extent the integrated power device 100 is structurally the same as the integrated power device 1 of Figure 1, the same reference numbers have been used, and the device will not be described any further. The ignition coil 101 is made up of a primary winding 101a and a secondary winding 101b. A first terminal 101c of the primary winding 101a and secondary winding 101b is connected to a supply line 102 set at a supply voltage V_B; a

second terminal 103 of the primary winding 101a is connected to the collector terminal of the power transistor 2; and a second terminal 104 of the secondary winding 101b is connected to a spark plug 105. In addition, the input terminal 3b of the driving circuit 3 is connected to a driving control unit 112 comprising known circuits that generate the driving signal S.

As is shown in Figure 5, the integrated power device 100 is made up of a first chip 106 integrating the power transistor 2 and a second chip 107 integrating the control circuit 3. To the extent the first chip 106 and the second chip 107 are structurally the same as the first chip 60 and second chip 61 of Figure 2, the same reference numbers have been used, and the chips will not be further described herein. In particular, the second chip 107 is implemented, as in the case of the second chip 61, using a high-voltage technology, for example M1 technology.

According to the present invention, the integrated power device 100 is assembled using the chip-on-chip solution, i.e., fixing the second chip 107 on top of the first chip 106. In particular, the second substrate 31 of the control circuit 3 is bonded on the metal emitter-contact region 14 of the power transistor 2 by means of an adhesive layer 108 which also creates an insulation between these two regions. In addition, formed on the surface 8a of the first chip 106, on top of the second annular region 19 (which replaces the metallization region 23), is a contact pad 109 having a first contact portion 109a which is in electrical contact with the second end 21b of the Zener diode 21, and a second contact portion 109b which is in electrical contact with the equipotential portion 8′ schematically represented by means of the intermediate node 24 that is connected to the collector region 6 of the power transistor 2 through the first diode 25 and to the metal emitter-contact region 14 through the second diode 26. The contact pad 109 is soldered by means of a wire 110 to an electrical connection region 111 formed on the surface 32a of the second chip 107 (see Figure 6) on top of the high-voltage region 30. In this way, an electrical connection is obtained between the high-voltage region 30 of the control circuit 3 and the collector region 6 of the power transistor 2 (which in known chip-on-chip solutions was not present), thus

enabling control of the collector voltage Vc applied to the collector region 6 by the control circuit 3.

Operation of the integrated power device 100 is described in what follows with reference to Figures 4 and 5. When the collector voltage Vc assumes positive values (charging phase of the ignition coil 101), the first diode 25 is forward-biased, whilst the second diode 26 is reverse-biased because on the emitter-contact region 14 an emitter voltage Ve is present equal to the ground voltage V_{GND}, namely, 0 V. In these conditions, there is present on the intermediate node 24 and hence on the contact pad 109 a first biasing voltage Vp1 equal to:

$$Vp1 = Vc - Vbe1$$

where Vbe1 is the voltage present across the first diode 25. The first biasing voltage Vp1 is applied to the electrical connection region 111, and hence to the high-voltage region 30 of the control circuit 3, via the wire 110.

Instead, when the collector voltage Vc assumes negative values (discharge phase of the ignition coil 101), the second diode 26 is forward-biased and connects the intermediate node 24 to the emitter-contact region 14 of the power transistor 2. In these conditions, there is present, on the intermediate node 24, and hence on the contact pad 109, a second biasing voltage Vp2 equal to:

$$Vp2 = Ve - Vbe2$$
$$Vp2 = Vc - Vbe2$$

where Vbe2 is the voltage present across the second diode 26, and $Ve = V_{GND} = 0$ V. In addition, the first diode 25 is reverse-biased thus insulating the intermediate node 24 from the collector region 6. In these conditions, the collector voltage Vc may assume even high negative values without causing flow of a high current in the control circuit 3, thus preventing destruction of the latter as occurs, instead, in known solutions, in so far as the collector region 6 and the high-voltage region 30 are completely insulated.

In addition, if the collector voltage Vc reaches a negative value equal to the breakdown voltage of the first diode 25, the latter operates as a Zener diode which is able to absorb a high energy compatible with the working conditions required in the applications of the integrated power device 100.

The advantages that may be obtained with the integrated power device 100 are described in what follows. In the first place, the integrated power device 100 according to the invention is particularly suited for being used in electronic ignition systems due to its capacity for carrying out efficient control of the collector voltage Vc (in fact, the control circuit 3 can perform control of the collector voltage Vc without being subject to the negative-voltage peaks of the latter), and due to its small overall dimensions (in so far as it does not require any external components to absorb the energy returned by the ignition coil 101 during the discharge phase of the latter). In existing electronic ignition systems, small overall dimensions prove particularly important in that the ignition coil and the integrated power device are mounted directly on the spark plug.

Finally, it is clear that numerous modifications and variations may be made to the integrated power device described and illustrated herein, all falling within the scope of the inventive idea, as defined in the attached claims and the equivalents thereof.

For example, the control circuit 3 may be built using a high-voltage BCD technology.